WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a logic circuit including a plurality of MIS transistors;

a first switch connected between an operating voltage supply point of the MIS transistor in said logic circuit and a power line;

a memory array including a plurality of static memory cells; and

a control circuit changing the substrate voltage of the MIS transistor constructing said memory cell according to its state.

2. The semiconductor device according to claim 1, wherein said plurality of MIS transistors have an N channel type MIS transistor and a P channel type MIS transistor,

the gates and the drains of said N channel type MIS transistor and said P channel type MIS transistor are connected.

3. The semiconductor device according to claim 1, further comprising a control circuit changing the substrate voltage of the MIS transistor in said logic circuit according to its state.

4. The semiconductor device according to claim 3, further comprising a second switch connected between the operating voltage supply point of the MIS transistor constructing said memory cell and the power line, wherein

a control circuit changing the substrate voltage of the MIS transistor constructing said first switch, said

second switch and said memory cell according to its state and a control circuit changing the substrate voltage of the MIS transistor in said logic circuit according to its state are constructed by the MIS transistor, respectively,

the film thickness of the insulating film of the MIS transistor constructing said first switch is larger than that of the insulating film of the MIS transistor constructing said second transistor.

5. The semiconductor device according to claim 4, further comprising a circuit controlling said memory cell array and a third switch changing the operating voltage of said control circuit according to its state, wherein

said memory array is divided into blocks and said third switch controls the operating voltage for each of the blocks.

6. The semiconductor device according to claim 3, wherein

the gate is controlled so that the MIS transistor constructing said first transistor is in the off state in a first state and is in the on state in a second state,

the control circuit changing the substrate voltage of the MIS transistor in said logic circuit according to its state controls the substrate voltage of the MIS transistor in said logic circuit so that an electric current flowing to the source-drain path of said MIS transistor in said first state is smaller than an electric current flowing to said second state,

the control circuit changing the substrate voltage of the MIS transistor constructing said memory cell

according to its state controls the substrate voltage of the MIS transistor in said memory cell so that an electric current flowing to the source-drain path of said MIS transistor in said first state is smaller than an electric current flowing to said second state.

7. A semiconductor device comprising:

a first memory cell having a first MIS transistor, a second MIS transistor, a third MIS transistor and a fourth MIS transistor, which are of an N channel type;

a second memory cell having a fifth MIS transistor, a sixth MIS transistor, a seventh MIS transistor and an eighth MIS transistor, which are of an N channel type,

wherein the gate-insulating film thickness of said first MIS transistor is smaller than that of said fifth MIS transistor.

8. The semiconductor device according to claim 7, further comprising:

a ninth MIS transistor in an input/output circuit;

a logic circuit having a tenth MIS transistor, wherein

the gate-insulating film thickness of said ninth MIS transistor is larger than that of said first MIS transistor,

the gate-insulating film thickness of said tenth MIS transistor is smaller than that of said fifth MIS transistor.

9. The semiconductor device according to claim 7, further comprising:

an input/output circuit; and

a logic circuit, wherein

the gate-insulating film thickness of the MIS transistor in said logic circuit is equal to that of said first MIS transistor,

the gate-insulating film thickness of the MIS transistor in said input/output circuit is equal to that of said fifth MIS transistor,

said first memory cell has a ninth MIS transistor and a tenth MIS transistor, which are of a P channel type,

said second memory cell has an eleventh MIS transistor and a twelfth MIS transistor, which are of a P channel type,

the gates of said third MIS transistor and said fourth MIS transistor are connected to a wordline, the gate of said first MIS transistor is connected to said fourth MIS transistor, the drain thereof is connected to said third MIS transistor, the gate of said second MIS transistor is connected to said third MIS transistor, and the drain thereof is connected to said second MIS transistor,

the gates of said seventh MIS transistor and said eighth MIS transistor are connected to a wordline, the gate of said fifth MIS transistor is connected to said eighth MIS transistor, the drain thereof is connected to said seventh MIS transistor, the gate of said sixth MIS transistor is connected to said seventh MIS transistor, and the drain thereof is connected to said eighth MIS transistor.

10. The semiconductor device according to claim 7, further

comprising:

a ninth MIS transistor having a source-drain path between the operating voltage supply point of said first memory cell and the power line,

wherein said ninth MIS transistor is controlled so as to be in the off state in a first state and to be in the on state in a second state,

before said second state is changed to said first state, information of said first memory cell is stored into said second memory cell.

11. A semiconductor device comprising:

a plurality of memory cells arranged at the cross point of a plurality of wordlines and bitlines;

a read/write control circuit connected to said bitline;

a decoder selecting said wordline;

a first switch connected between said decoder and a first node; and

a second switch connected between said read/write control circuit and a second node.

12. The semiconductor device according to claim 11, wherein said first switch has a first MIS transistor of a P channel type having a source-drain path connected between said decoder and said first node,

said second switch has a second MIS transistor of an N channel type having a source-drain path connected between said read/write control circuit and said second node.

13. The semiconductor device according to claim 12, further

comprising:

a logic circuit having a plurality of MIS transistors;

a third MIS transistor having a source-drain path between the operating voltage point of said MIS transistor and the power line,

wherein the gate-insulating film thickness of said third MIS transistor is larger than that of said first MIS transistor.

14. The semiconductor device according to claim 11, wherein said plurality of memory cells are divided into blocks and each of the blocks has a switch controlling the operating voltage of said memory cell.

15. The semiconductor device according to claim 14, further comprising:

an input/output circuit,

wherein the gate-insulating film thickness of the MIS transistor in said input/output circuit is larger than that of the MIS transistor constructing said switch controlling the operating voltage.